I/O CIRCUITRY SHARED BETWEEN PROCESSOR AND PROGRAMMABLE LOGIC PORTIONS OF AN INTEGRATED CIRCUIT

ABSTRACT OF THE DISCLOSURE

The present invention provides circuitry and methods for sharing I/O pins between a programmable logic portion and an embedded processor portion of a chip. The circuits in the programmable logic portion and the embedded processor portion can access data signals from and send data signals to the same I/O pins. The data signals are multiplexed to control access to the shared I/O pins. The multiplexers may be controlled by a control signal that determines when particular I/O pins are accessed by the programmable logic portion and the embedded processor portion. Control signals that configure the associated I/O pin circuitry to the correct I/O standard are also multiplexed by the shared I/O circuitry of the present invention. Signals received at the shared I/O pins that are transmitted to the embedded processor portion may be concurrently sent to snoop circuitry within the programmable logic portion.